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PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Toru KAWASAKI — Appeal No. _____

Application No. 10/657,236 — Group 2811

Filed September 9, 2003 — Examiner Sara W. CRANE

SOLID STATE IMAGE SENSOR HAVING PLANARIZED STRUCTURE UNDER LIGHT SHIELDING METAL LAYER

APPEAL BRIEF

MAY IT PLEASE YOUR HONORS:

1. Real Party in Interest

The real party in interest in this Appeal is the Assignee, NEC Electronics Corporation of Kanagawa, Japan.

2. Related Appeals and Interferences

None.

3. Status of the Claims

Claims 30-40 are pending from whose final rejection this appeal is taken. Claim 40 was withdrawn from consideration as being directed to a non-elected species. Claims 1-29 were previously canceled.

4. Status of Amendments

No amendment was filed subsequent to the final rejection of the claims on appeal.

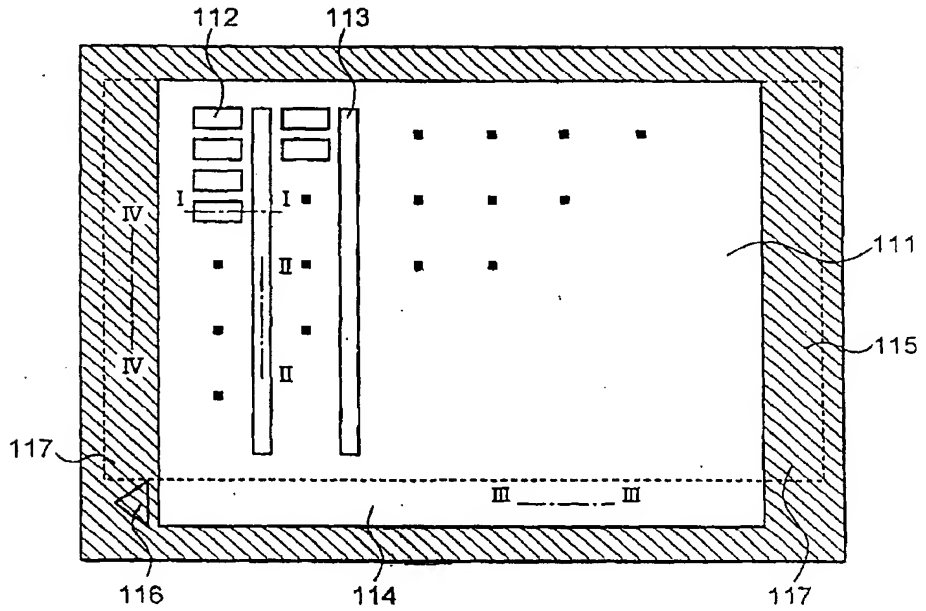
5. Summary of Claimed Subject Matter

With reference to page 1, lines 7-9 of the specification, the invention relates to a solid state image sensor, and particularly to a solid state image sensor having a planarized structure under a light shielding metal layer.

Claim 30 is the only independent claim.

Claim 30 recites a solid state image sensor illustrated by way of example in Figure 6, reproduced below. The solid state image sensor includes an image area 111 and a peripheral area 115.

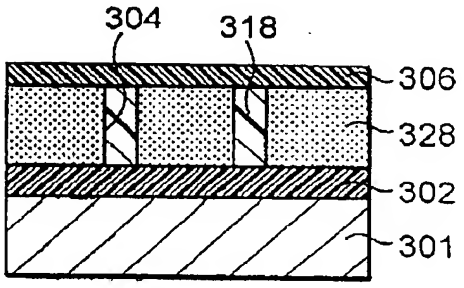
FIG. 6



As further illustrated by way of example in Figures 15B and 15C, reproduced below, claim 30 recites a first insulating layer 318, 306 covering a plurality of shift register electrodes

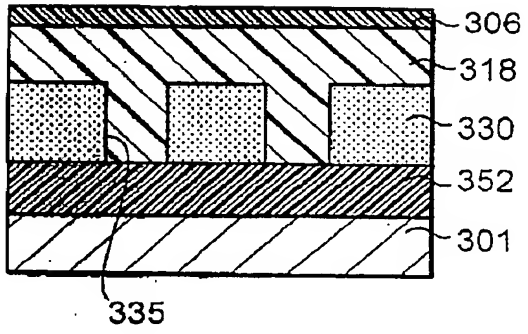
328 (of the image area) and filling a first gap 304 between adjacent shift register electrodes. The first insulating film 318, 306 has a first thickness over an upper surface of each of the shift register electrodes 328. Page 15, lines 17-23 disclose film 318 filling the first gap 304. Page 17, lines 12-14 disclose film 306.

FIG. 15B



Claim 30 also recites a second insulating layer 318, 306 covering a plurality of peripheral electrodes 330 and filling a second gap 335 between adjacent peripheral electrodes 330. The second insulating film 318, 306 has a second thickness larger than the first thickness.

FIG. 15C



Page 15, lines 27-31 disclose filling the second gap 335. Page 18, line 7 to page 19, line 6 disclose the formation of the films 318, 306 such that the second insulating film 318, 306

covering the peripheral electrodes 330 is thicker than the first insulating film 318, 306 covering the shift register electrodes 328.

As disclosed on specification page 26, lines 7-27, filling the gaps between electrodes and creating a planarized surface in the imaging area, while keeping the insulating material in the peripheral area at a larger height permits a light shielding metal layer to be formed without producing discontinuity, which reduces smear brightness. The thicker film in the peripheral area also reduces parasitic capacitance, resulting in a reduction of device power consumption.

6. Ground of Rejection to be Reviewed on Appeal

The sole issue on appeal is whether claims 30-39 would have been obvious, in the meaning of 35 USC §103(a) over Applicant's disclosed prior art in view of HATANO 6,143,585.

7. Arguments

The final rejection argues (page 2, lines 13-17) that HATANO is only relied upon for the disclosure of a thicker peripheral region. The final rejection concludes that it would have been obvious to have a thicker peripheral region to resist higher voltages that are applied to such peripheral region.

However, this conclusion is believed to be untenable for at least the following reasons.

First, this conclusion disregards the claimed invention as a whole.

Claim 30 recites a second insulating layer covering peripheral electrodes and filling a second gap. The second insulating layer has a second thickness over an upper surface of each of the peripheral electrodes and the second thickness is larger than a first thickness of a first insulating layer (covering shift register electrodes in an imaging area).

As seen by comparing Figures 15B and 15C, reproduced on page 3 above, with prior art Figures 4B and 4C, reproduced below, the main purpose of having a thicker second insulating layer is not to increase the thickness of the peripheral area, but to ensure that the gaps 335 are filled.

FIG. 4B

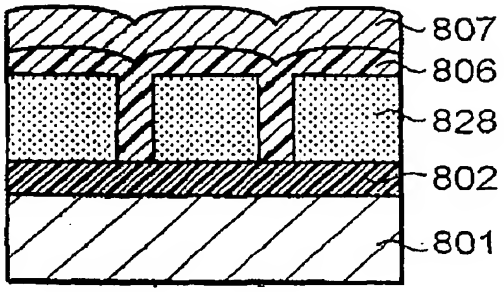
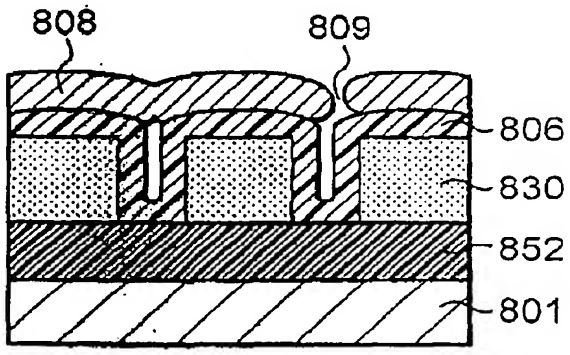


FIG. 4C



In Figure 4C, it is seen that the gap between peripheral electrodes 830 is not filled by insulating layer 806, which leads to discontinuity 809 in the overlying metal layer, which undesirably increases smear brightness.

However, as seen in the Figures, the peripheral area of Figure 4C is already thicker than the imaging area of Figure 4B based on the thicknesses of films 802 and 852. Page 2, lines 20-22 disclose that a step portion is created between film 802 and dielectric 852. Thus, the prior art Figures already disclose forming a thicker peripheral region before the electrodes are formed.

Similarly, Figure 5D of HATANO, reproduced below, discloses forming a thicker insulating layer 406 in the peripheral area before electrodes (wiring 412) is formed.

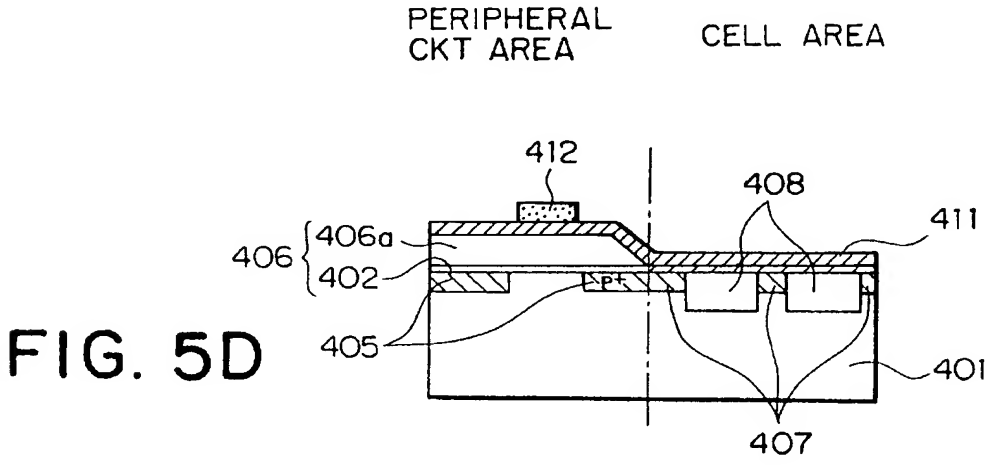


FIG. 5D

Thus, the prior art perceived a need to form a thicker peripheral area before the electrodes were formed, whereas the present inventor eliminated gaps between electrodes by forming a

thicker insulating layer over the electrodes, while still having the thicker area below the electrodes.

In the disclosed embodiment, the present inventor overcame the shortcomings of the prior art by performing a two-step process of filling the gaps with a first insulating material, then planarizing only the imaging area, and then forming a second insulating layer. Since the peripheral area was not planarized, the insulation over the electrodes in the peripheral area is thicker than that over the electrodes in the imaging area.

The proposed combination of references does not provide any insight to achieve such structure. Rather, the disclosed prior art discloses a single uniform thickness insulating layer over the electrodes, and HATANO discloses a thicker insulating layer below the electrodes. Thus, when the claimed invention is considered as a whole, the recited structure would not have been obvious to those skilled in the art.

Second, the final rejection has failed to establish *prima facie* obviousness, because the prior art references or combination of references does not teach or suggest all the limitations of the claims.

The final rejection recognizes that applicant's disclosed prior art Figures 4B and 4C do not disclose a thicker insulating layer covering peripheral electrodes and offers HATANO for this feature.

However, the thicker insulating layer in the peripheral area of HATANO is over ion implantation region 305 (of Figure 4E) or 405 (of Figure 5D), not over peripheral electrodes.

Column 7, lines 13-17 of HATANO teach that after the thicker insulating layer 309 is formed, electrodes for transferring signal charges, an interlayer insulating film and other elements are formed to complete the device.

Thus, the electrodes of HATANO are formed after the thicker insulating layer is formed. HATANO does not teach or suggest forming an insulating layer over an upper surface of the peripheral electrodes. As each of the references fails to suggest forming a thicker insulating layer over an upper surface of peripheral electrodes, *prima facie* obviousness has not been established.

Third, the final rejection is impermissibly picking and choosing only so much from the references that support the position in the final rejection, to the exclusion of other parts necessary to the full appreciation of what the references fairly suggest to one of ordinary skill in the art.

As seen in disclosed prior art Figures 3B and 3C, reproduced below, and as disclosed on specification page 2, line 30 to page 3, line 1, a single substantially uniform thickness insulating layer 806 is applied over the entire structure to cover the electrodes in the imaging area and the peripheral area.

FIG. 3B

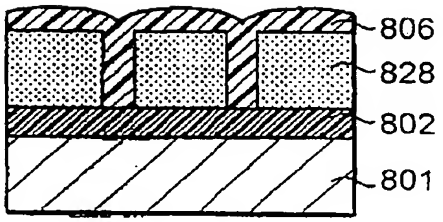
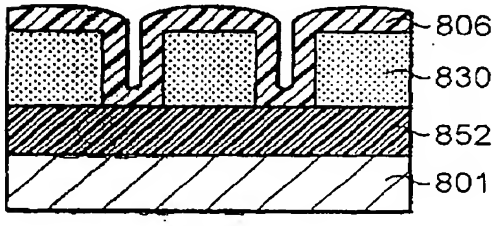


FIG. 3C



The figures of HATANO show a single insulating layer covering a planar area over a substrate that does not include any electrodes. HATANO neither discloses forming an insulating layer on a non-planar area (covering electrodes) nor that such insulating layer fills a gap between electrodes. As HATANO discloses forming a thicker insulating layer before the electrodes are formed, HATANO teaches away from forming a thicker insulating layer over the electrodes.

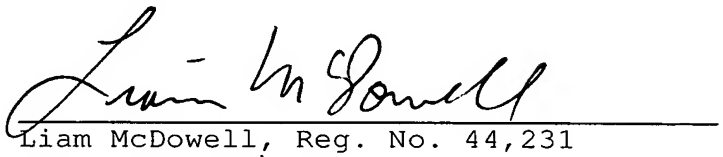
Accordingly, the references do not fairly suggest forming a thicker insulating layer on peripheral electrodes. Instead, their combination teaches away from such structure. Therefore, absent impermissible hindsight reasoning it would not have been obvious to form a thicker insulating layer covering peripheral electrodes.

Conclusion

Appellant respectfully urges that the rejection on appeal should not be maintained and respectfully requests that this rejection be reversed.

Respectfully submitted,

YOUNG & THOMPSON



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December 27, 2006

8. Claims Appendix:

30. A solid state image sensor comprising:

a semiconductor substrate having an imaging area and a peripheral area;

a plurality of shift register electrodes formed on said imaging area with a first gap between adjacent ones of said shift register electrodes, each of said shift register electrodes being elongated over said peripheral area, a plurality of peripheral electrodes being thereby formed on said peripheral area with a second gap between adjacent ones of said peripheral electrodes;

a first insulating layer covering said shift register electrodes and filling said first gap, said first insulating layer having a first thickness over an upper surface of each of said shift register electrodes; and

a second insulating layer covering said peripheral electrodes and filling said second gap, said second insulating layer having a second thickness over an upper surface of each of said peripheral electrodes, said second thickness being larger than said first thickness.

31. The solid state image sensor as claimed in claim 30, wherein said first insulating layer includes first and second insulating portions, the first insulating portion filling said first gap to a level of said upper surface of each of said shift register electrodes and said second insulating portion being

formed on said first insulating portion and said upper surface of each of said shift register electrodes, and said second insulating layer includes third and fourth insulating portions, said third insulating portion filling said second gap and being extended over said upper surface of each of said peripheral electrodes and said fourth insulating portion being formed on said third insulating portion.

32. The solid state image sensor as claimed in claim 31, wherein said second insulating portion has said first thickness, said third insulating portion having a third thickness over said upper surface of each of said peripheral electrodes, and said fourth insulating portion having said first thickness to thereby cooperate with said third insulating portion to provide said second thickness.

33. The solid state image sensor as claimed in claim 31, wherein said first and third insulating portions include thermally reflowable material.

34. The solid state image sensor as claimed in claim 33, wherein said thermally reflowable material is Boro-Phosphorous-Silicate-Glass (BPSG).

35. The solid state image sensor as claimed in claim 30, wherein a width of said second gap is longer than a width of said first gap.

36. The solid state image sensor as claimed in claim 30, wherein said plurality of shift register electrodes functions as a plurality of vertical and horizontal shift register electrodes, one of said plural shift register electrodes functions as either a vertical shift register electrode or a horizontal shift register electrode.

37. The solid state image sensor as claimed in claim 31, further comprising a plurality of photoelectric conversion elements formed in said imaging area, said second insulating portion extended over said plurality of photoelectric conversion elements, an upper surface of said second insulating portion over each of said plurality of photoelectric conversion elements being lower than said upper surface of each of said plurality of shift register electrodes.

38. The solid state image sensor as claimed in claim 30, further comprising a light shielding metal layer provided on said first and second insulating layer, said light shielding metal layer serving as interconnects for making electrical connection to said plurality of peripheral electrodes.

39. The solid state image sensor as claimed in claim 36, wherein said plurality of vertical and horizontal shift register electrodes is made from a single layer of conductor.

40. The solid state image sensor as claimed in claim 36, wherein each of said vertical and horizontal shift register electrodes has a silicide layer at a surface portion of each of said vertical and horizontal shift register electrodes.

9. Evidence Appendix

None.

10. Related Proceedings Appendix

None.